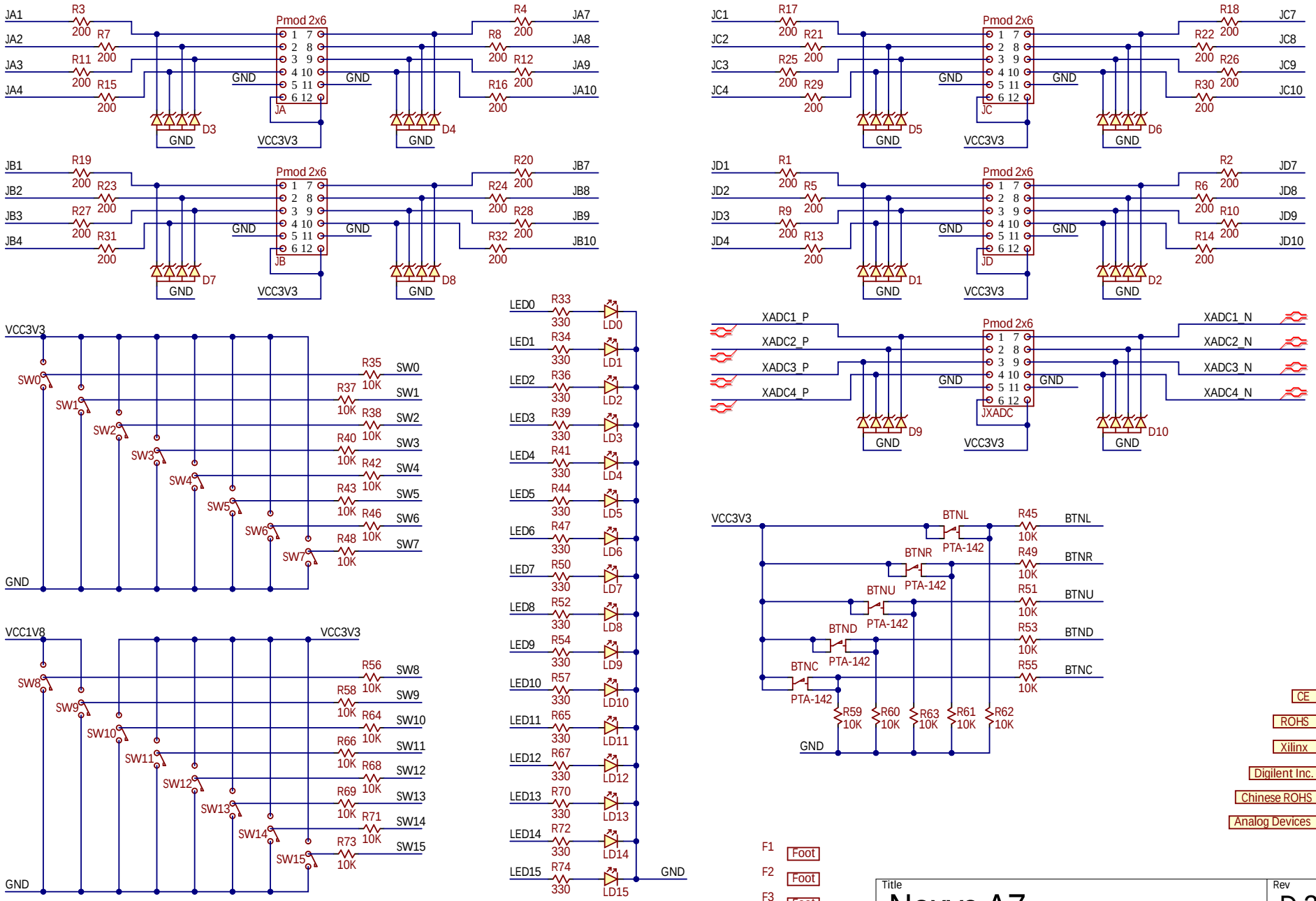

Title	Nexys A7
Rev	D.3
Circuit	PMOD, I/O
Doc#	500-292
Engineer	EG
Author	DL
Date	1/25/2022
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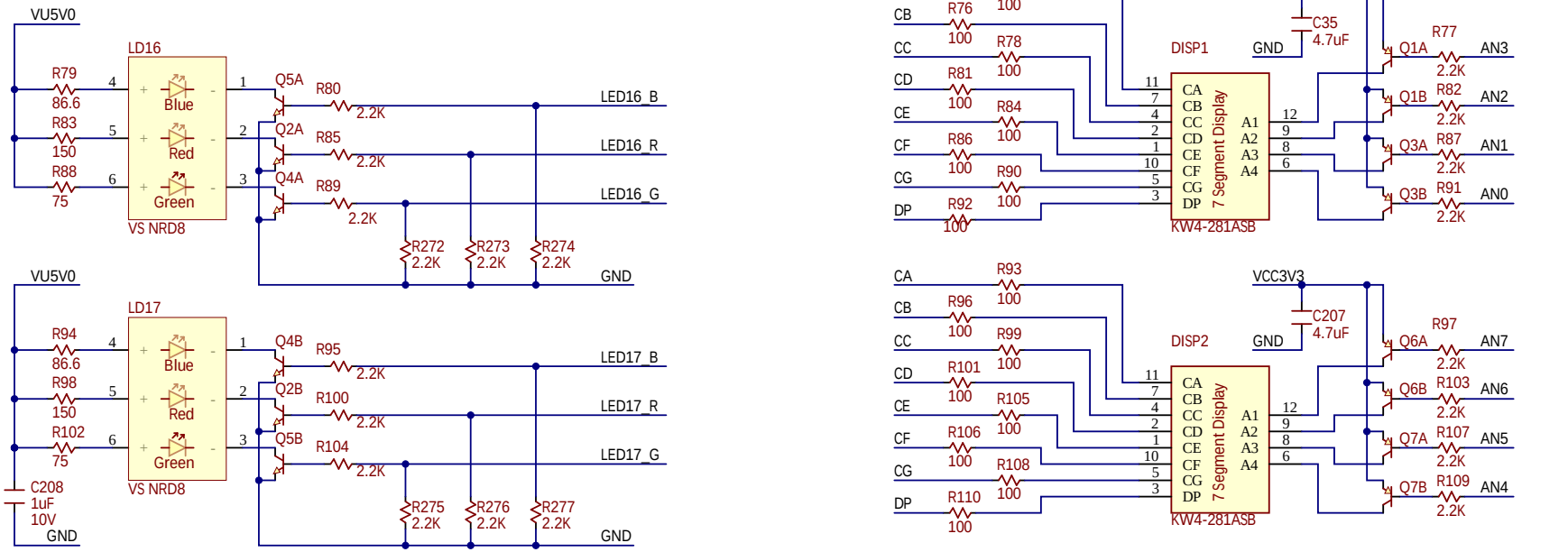

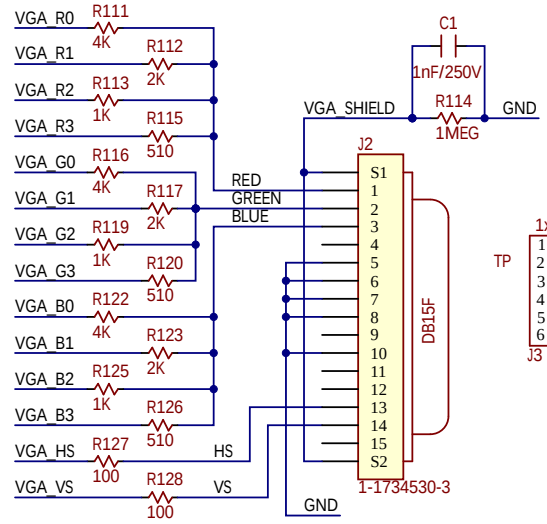

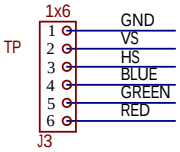

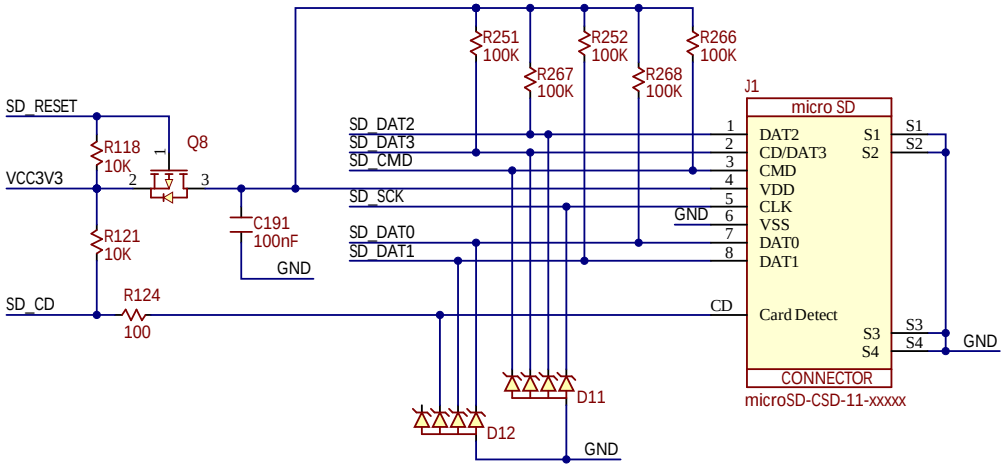

Title	Nexys A7
Rev	D.3
Circuit	7 SEG, VGA, SD
Doc#	500-292
Engineer	EG
Author	DL
Date	1/25/2022
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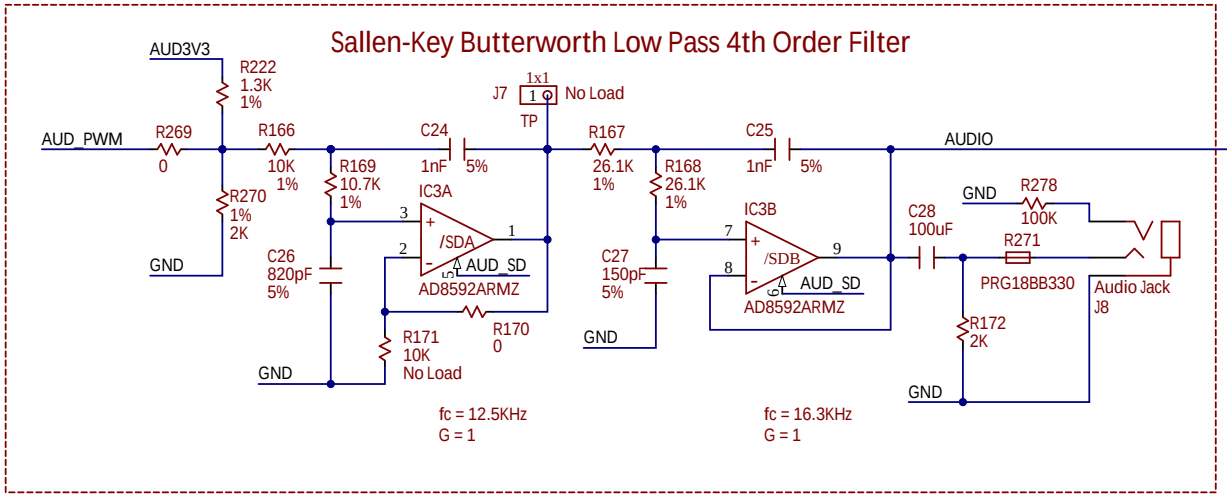

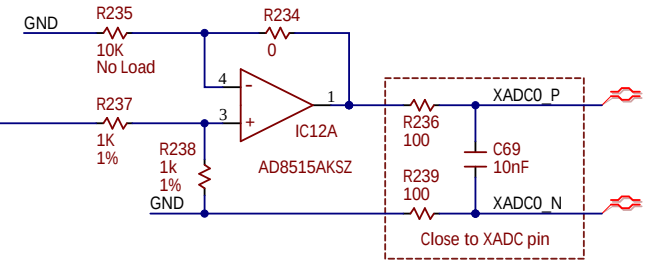

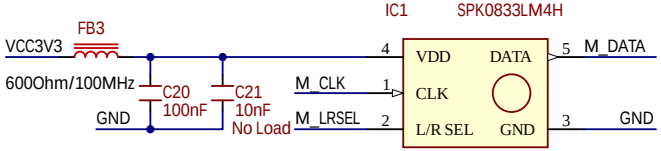

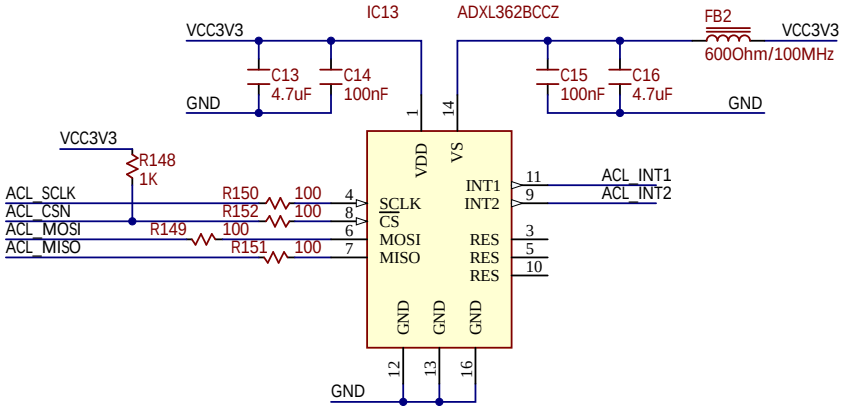

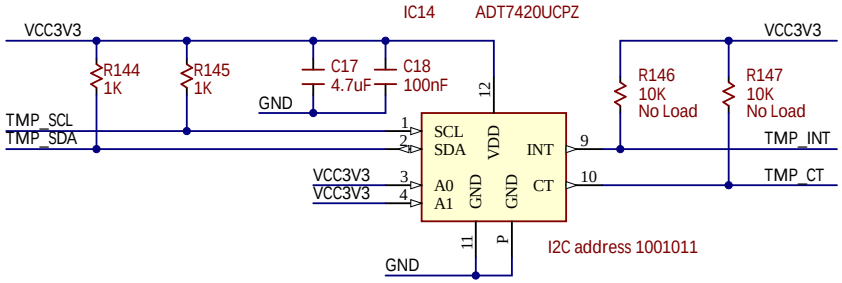

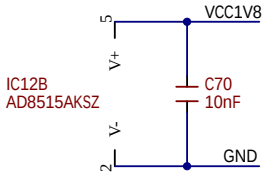

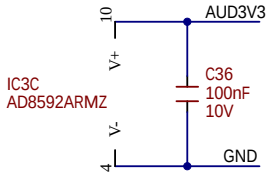

For more information on the parts used in this design, please refer to:

http://www.analog.com/ad8592 (CMOS Single Supply RRIO Dual Op Amp with±250 mA Output Current and Shutdown Mode)

http://www.analog.com/ad8515 (1.8 V Low Power CMOS Rail-to-Rail Input/Output Operational Amplifier)

http://www.analog.com/adxl362 (Micropower, 3-Axis, ±2 g/±4 g/±8 g Digital Output MEMS Accelerometer)

http://www.analog.com/adt7420 (±0.25°C Accurate, 16-Bit Digital I2C Temperature Sensor)

Title	Rev
Nexys A7	D.3

Circuit	ETH, TMP, ACL,AUDIO
Doc#	500-292
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Author	DL
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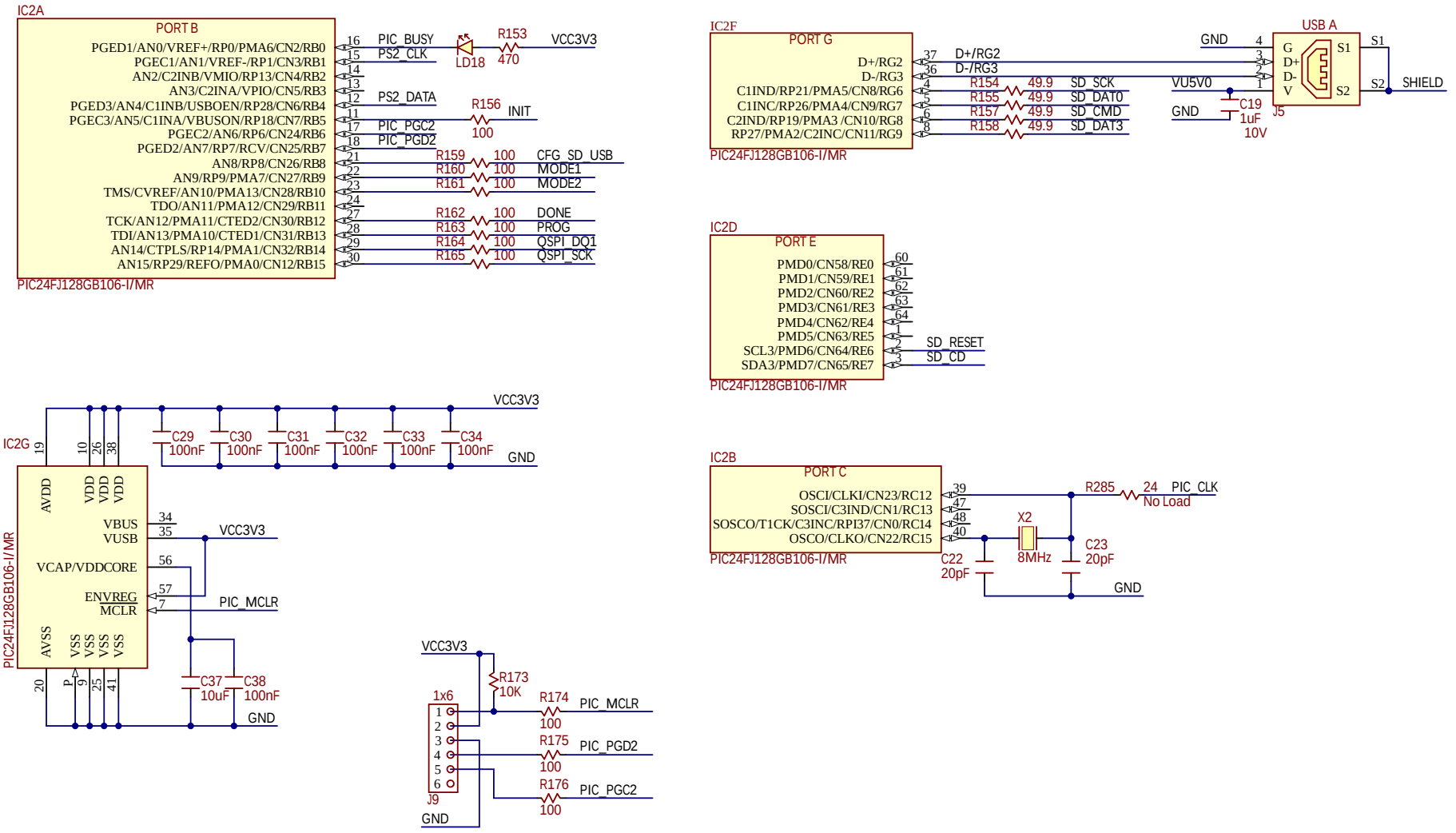

Title	Nexys A7
Rev	D.3
Circuit	USB HID
Doc#	500-292
Engineer	EG
Author	DL
Date	1/25/2022
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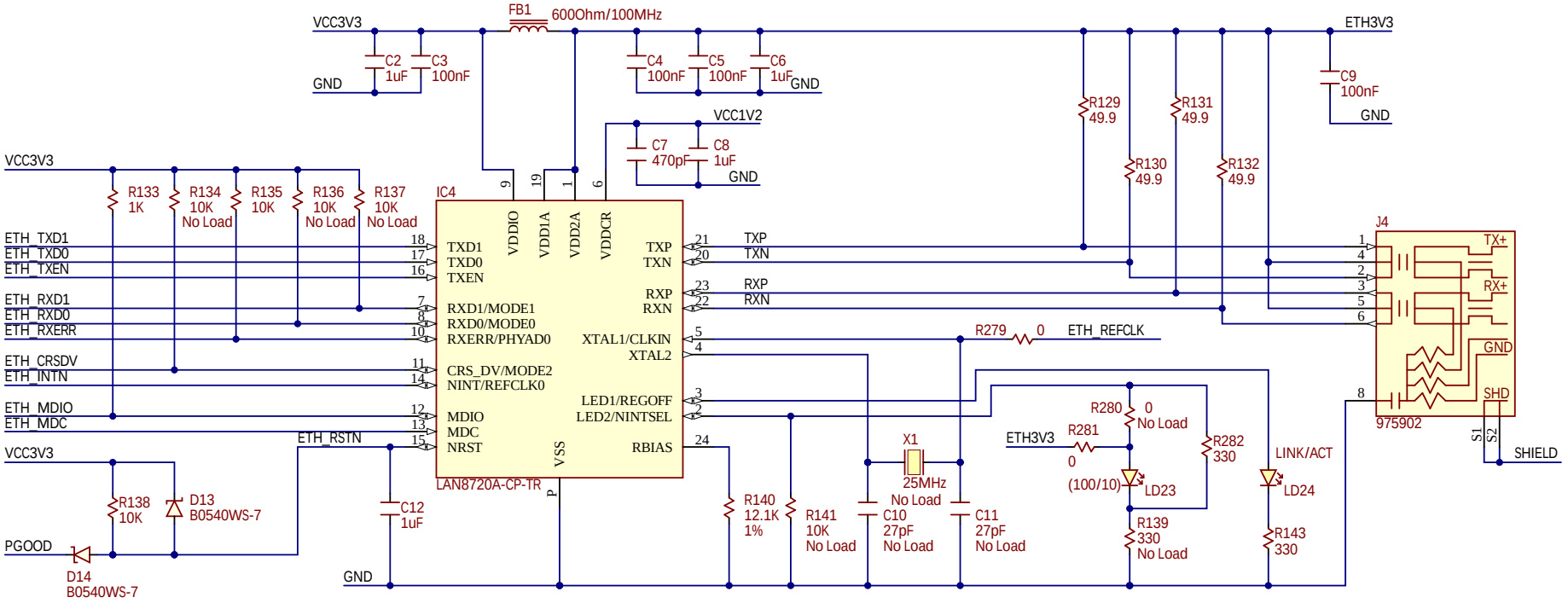

NOTE: REF_CLK In Mode (ETH_REFCLK = 50MHz)

Title	Nexys A7
Rev	D.3
Circuit	ETHERNET
Doc#	500-292
Engineer	EG
Author	DL
Date	1/25/2022
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Title	Nexys A7
Rev	D.3
Circuit	USB PROG/UART
Doc#	500-292
Engineer	EG
Author	DL
Date	1/25/2022
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For the -50T variant: IC8=XC7A50T-1CSG324I

IC8A — BANK 14

LED17_G R11	IO_0_14	L18 CG
CB R10	IO_25_14	M18 BTNU
	IO_L4P_T0_D04_14	R12 LED16_B
	IO_L4N_T0_D05_14	R13 SW7
	IO_L5P_T0_D06_14	M13 SW2
	IO_L5N_T0_D07_14	R18 LED4
	IO_L6N_T0_D08_VREF_14	T18 SW5
	IO_L7P_T1_D09_14	N14 LED3
	IO_L7N_T1_D10_14	P14 AN4
	IO_L8P_T1_D11_14	N17 BTNC
	IO_L8N_T1_D12_14	P18 BTND
	IO_L9P_T1_DQS_14	M16 LED16_G
	IO_L9N_T1_DQS_D13_14	M17 BTNR
	IO_L10P_T1_D14_14	N15 LED16_R
	IO_L10N_T1_D15_14	N16 LED17_R
	IO_L11P_T1_SRCC_14	P17 BTNL
	IO_L11N_T1_SRCC_14	R17 SW4
	IO_L12P_T1_MRCC_14	P15 CE
	IO_L12N_T1_MRCC_14	R15 SW3
	IO_L13P_T2_MRCC_14	T14 AN5
	IO_L13N_T2_MRCC_14	T15 LED9
	IO_L14P_T2_SRCC_14	V16 LED8
	IO_L14N_T2_SRCC_14	U17 LED6
	IO_L16N_T2_A15_D31_14	U18 SW6
	IO_L17P_T2_A14_D30_14	U16 LED7
	IO_L17N_T2_A13_D29_14	V17 LED5
	IO_L18P_T2_A12_D28_14	T11 CF
	IO_L18N_T2_A11_D27_14	U11 SW14
	IO_L19P_T3_A10_D26_14	U12 SW13
	IO_L19N_T3_A09_D25_VREF_14	V12 LED14
	IO_L20P_T3_A08_D24_14	V10 SW15
	IO_L20N_T3_A07_D23_14	V11 LED15
	IO_L21P_T3_DQS_14	U14 LED10
	IO_L21N_T3_DQS_A06_D22_14	V14 LED13
	IO_L22P_T3_A05_D21_14	T13 SW11
	IO_L22N_T3_A04_D20_14	U13 AN7
	IO_L23P_T3_A03_D19_14	V9 AN2
	IO_L23N_T3_A02_D18_14	T10 CA
	IO_L24P_T3_A01_D17_14	
	IO_L24N_T3_A00_D16_14	

XC7A100T-1CSG324C

IC8B — BANK 15

JB9 G13	IO_0_15	D14 JB1
CC K16	IO_25_15	C14 TMP_SCL
	IO_L1P_T0_AD0P_15	B13 ACL_INT1
	IO_L1N_T0_AD0N_15	B14 TMP_CT
	IO_L2P_T0_AD8P_15	C12 CPU_RESETN
	IO_L2N_T0_AD8N_15	B12 VGA_VS
	IO_L3P_T0_DQS_AD1P_15	B11 VGA_HS
	IO_L3N_T0_DQS_AD1N_15	A11 AUD_PWM
	IO_L4P_T0_15	F13 JB8
	IO_L4N_T0_15	F14 ACL_MOSI
	IO_L5P_T0_AD9P_15	D12 AUD_SD
	IO_L5N_T0_AD9N_15	D13 TMP_INT
	IO_L6P_T0_15	B16 XA3_P
	IO_L6N_T0_VREF_15	B17 XA3_N
	IO_L7P_T1_AD2P_15	A15 XA2_P
	IO_L7N_T1_AD2N_15	A16 XA2_N
	IO_L8P_T1_AD10P_15	A13 XA1_P
	IO_L8N_T1_AD10N_15	A14 XA1_N
	IO_L9P_T1_DQS_AD3P_15	B18 XA4_P
	IO_L9N_T1_DQS_AD3N_15	A18 XA4_N
	IO_L10P_T1_AD11P_15	E15 ACL_MISO
	IO_L10N_T1_AD11N_15	E16 JB7
	IO_L11P_T1_SRCC_15	D15 ACL_CSN
	IO_L11N_T1_SRCC_15	C15 TMP_SDA
	IO_L12P_T1_MRCC_15	H16 JB10
	IO_L12N_T1_MRCC_15	G16 JB3
	IO_L13P_T2_MRCC_15	F15 ACL_SCLK
	IO_L13N_T2_MRCC_15	F16 JB2
	IO_L14P_T2_SRCC_15	H14 JB4
	IO_L14N_T2_SRCC_15	G14 LED17_B
	IO_L15P_T2_DQS_15	E17 JA8
	IO_L15N_T2_DQS_ADV_B_15	D17 JA7
	IO_L16P_T2_A28_15	K13 CD
	IO_L16N_T2_A27_15	J13 LED2
	IO_L17P_T2_A26_15	H17 LED0
	IO_L17N_T2_A25_15	G17 JA4
	IO_L18P_T2_A24_15	J14 AN3
	IO_L18N_T2_A23_15	H15 DP
	IO_L19P_T3_A22_15	C16 ACL_INT2
	IO_L19N_T3_A21_VREF_15	C17 JA1
	IO_L20P_T3_A20_15	E18 JA3
	IO_L20N_T3_A19_15	D18 JA2
	IO_L21P_T3_DQS_15	G18 JA10
	IO_L21N_T3_DQS_A18_15	F18 JA9
	IO_L22P_T3_A17_15	J17 AN0
	IO_L22N_T3_A16_15	J18 AN1
	IO_L23P_T3_FOE_B_15	K15 LED1
	IO_L23N_T3_FWE_B_15	J15 SW0
	IO_L24P_T3_RS1_15	
	IO_L24N_T3_RS0_15	

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IC8D — BANK 34

DDR_CS K6	IO_0_34	L1 DDR_CAS
SW9 U8	IO_25_34	M1 DDR_CKE
	IO_L1P_T0_34	K3 DDR_A13
	IO_L1N_T0_34	L3 DDR_A4
	IO_L2P_T0_34	N2 DDR_WE
	IO_L2N_T0_34	N1 DDR_A7
	IO_L3P_T0_DQS_34	M3 DDR_ODT
	IO_L3N_T0_DQS_34	M2 DDR_A6
	IO_L4P_T0_34	K5 DDR_A11
	IO_L4N_T0_34	L4 DDR_A8
	IO_L5P_T0_34	L6 DDR_CK_P
	IO_L5N_T0_34	L5 DDR_CK_N
	IO_L6P_T0_34	U1 DDR_UDM
	IO_L6N_T0_VREF_34	V1 DDR_DQ14
	IO_L7P_T1_34	U4 DDR_DQ11
	IO_L7N_T1_34	U3 DDR_DQ9
	IO_L8P_T1_34	U2 DDR_UDQS_P
	IO_L8N_T1_34	V2 DDR_UDQS_N
	IO_L9P_T1_DQS_34	V5 DDR_DQ10
	IO_L9N_T1_DQS_34	V4 DDR_DQ12
	IO_L10P_T1_34	R3
	IO_L10N_T1_34	T3 DDR_DQ15
	IO_L11P_T1_SRCC_34	T5 DDR_DQ8
	IO_L11N_T1_SRCC_34	T4 DDR_DQ13
	IO_L12P_T1_MRCC_34	N5 DDR_A9
	IO_L12N_T1_MRCC_34	P5 DDR_A5
	IO_L13P_T2_MRCC_34	P4 DDR_A1
	IO_L13N_T2_MRCC_34	P3 DDR_BA1
	IO_L14P_T2_SRCC_34	P2 DDR_BA0
	IO_L14N_T2_SRCC_34	R2 DDR_A10
	IO_L15P_T2_DQS_34	M4 DDR_A0
	IO_L15N_T2_DQS_34	N4 DDR_RAS
	IO_L16P_T2_34	R1 DDR_BA2
	IO_L16N_T2_34	T1 DDR_A3
	IO_L17P_T2_34	M6 DDR_A2
	IO_L17N_T2_34	N6 DDR_A12
	IO_L18P_T2_34	R6 DDR_DQ5
	IO_L18N_T2_34	R5 DDR_DQ7
	IO_L19P_T3_34	V7 DDR_DQ4
	IO_L19N_T3_VREF_34	V6 DDR_DQ1
	IO_L20P_T3_34	U9 DDR_LDQS_P
	IO_L20N_T3_34	V9 DDR_LDQS_N
	IO_L21P_T3_DQS_34	U7 DDR_DQ3
	IO_L21N_T3_DQS_34	U6 DDR_DQ6
	IO_L22P_T3_34	R7 DDR_DQ0
	IO_L22N_T3_34	T6 DDR_LDM
	IO_L23P_T3_34	R8 DDR_DQ2
	IO_L23N_T3_34	T8 SW8
	IO_L24P_T3_34	
	IO_L24N_T3_34	

XC7A100T-1CSG324C

IC8E — BANK 35

M_LRSEL F5	IO_0_35	C6 VGA_G0
M_CLK J5	IO_25_35	C5 VGA_R2
	IO_L1P_T0_AD4P_35	B7 VGA_B0
	IO_L1N_T0_AD4N_35	B6 VGA_G2
	IO_L2P_T0_AD12P_35	A6 VGA_G3
	IO_L2N_T0_AD12N_35	A5 VGA_G1
	IO_L3P_T0_DQS_AD5P_35	D8 VGA_B3
	IO_L3N_T0_DQS_AD5N_35	C7 VGA_B1
	IO_L4P_T0_35	E6 JC10
	IO_L4N_T0_35	E5 UART_RTS
	IO_L5P_T0_AD13P_35	E7 JC7
	IO_L5N_T0_AD13N_35	D7 VGA_B2
	IO_L6P_T0_35	C4 UART_TXD_IN
	IO_L6N_T0_VREF_35	B4 VGA_R1
	IO_L7P_T1_AD6P_35	A4 VGA_R3
	IO_L7N_T1_AD6N_35	A3 VGA_R0
	IO_L8P_T1_AD14P_35	B1 SD_SCK
	IO_L8N_T1_AD14N_35	A1 SD_CD
	IO_L9P_T1_DQS_AD7P_35	B3 ETH_RSTN
	IO_L9N_T1_DQS_AD7N_35	B2 PS2_DATA
	IO_L10P_T1_AD15P_35	D5 ETH_REFCLK
	IO_L10N_T1_AD15N_35	D4 UART_RXD_OUT
	IO_L11P_T1_SRCC_35	E3 CLK100MHZ
	IO_L11N_T1_SRCC_35	D3 UART_CTS
	IO_L12P_T1_MRCC_35	F4 PS2_CLK
	IO_L12N_T1_MRCC_35	F3 JD10
	IO_L13P_T2_MRCC_35	E2 SD_RESET
	IO_L13N_T2_MRCC_35	D2 SD_DAT3
	IO_L14P_T2_SRCC_35	H2 JD7
	IO_L14N_T2_SRCC_35	G2 JD9
	IO_L15P_T2_DQS_35	C2 SD_DAT0
	IO_L15N_T2_DQS_35	C1 SD_CMD
	IO_L16P_T2_35	H1 JD2
	IO_L16N_T2_35	G1 JD3
	IO_L17P_T2_35	F1 SD_DAT2
	IO_L17N_T2_35	E1 SD_DAT1
	IO_L18P_T2_35	G6 JC4
	IO_L18N_T2_35	F6 JC2
	IO_L19P_T3_35	G4 JD8
	IO_L19N_T3_VREF_35	G3 JD4
	IO_L20P_T3_35	J4 JC9
	IO_L20N_T3_35	H4 JD1
	IO_L21P_T3_DQS_35	J3 JC8
	IO_L21N_T3_DQS_35	J2 JC3
	IO_L22P_T3_35	K2 AN6
	IO_L22N_T3_35	K1 JC1
	IO_L23P_T3_35	H6 SW12
	IO_L23N_T3_35	H5 M_DATA
	IO_L24P_T3_35	
	IO_L24N_T3_35	

XC7A100T-1CSG324C

IC8C — BANK 16

	IO_L6N_T0_VREF_16	D9 ETH_CRSDV
	IO_L11P_T1_SRCC_16	C9 ETH_MDC
	IO_L11N_T1_SRCC_16	B9 ETH_TXEN
	IO_L12P_T1_MRCC_16	B8 ETH_INTN
	IO_L12N_T1_MRCC_16	A8 ETH_TXD1
	IO_L13P_T2_MRCC_16	C11 ETH_RXD0
	IO_L13N_T2_MRCC_16	C10 ETH_RXERR
	IO_L14P_T2_SRCC_16	A10 ETH_TXD0
	IO_L14N_T2_SRCC_16	A9 ETH_MDIO
	IO_L19N_T3_VREF_16	D10 ETH_RXD1

XC7A100T-1CSG324C

XADC1_P — R200 100 — XA1_P
C60 1nF No Load
XADC1_N — R203 100 — XA1_N

XADC2_P — R201 100 — XA2_P
C61 1nF No Load
XADC2_N — R204 100 — XA2_N

XADC3_P — R202 100 — XA3_P
C62 1nF No Load
XADC3_N — R205 100 — XA3_N

XADC4_P — R206 100 — XA4_P
C63 1nF No Load
XADC4_N — R207 100 — XA4_N

IC9

VCC3V3 — 4 VDD — OUT 3 — CLK100MHZ
1 STBY — GND 2 — GND
C64 100nF
GND
DSC1033CC1-100.0000T

Title	Nexys A7
Rev	D.3
Circuit	FPGA BANKS
Doc#	500-292
Engineer	EG
Author	DL
Date	1/25/2022
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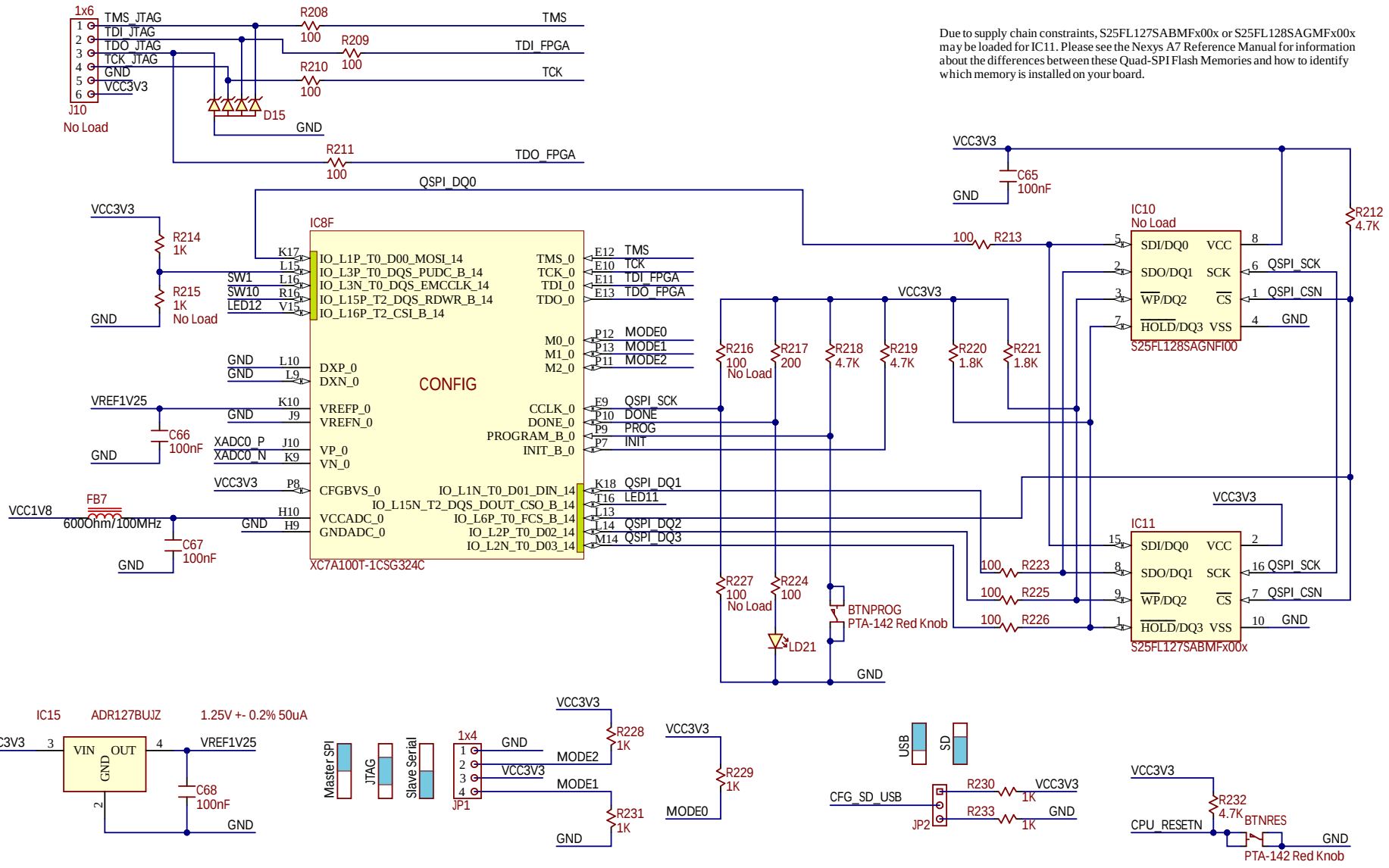

Due to supply chain constraints, S25FL127SABMFx00x or S25FL128SAGMFx00x may be loaded for IC11. Please see the Nexys A7 Reference Manual for information about the differences between these Quad-SPI Flash Memories and how to identify which memory is installed on your board.

For more information on the parts used in this design, please refer to:

http://www.analog.com/adr127 (Precision, Micropower LDO Voltage References in TSOT)

Title	Nexys A7
Rev	D.3
Circuit	CONFIG, SPI FLASH
Doc#	500-292
Engineer	EG
Author	DL
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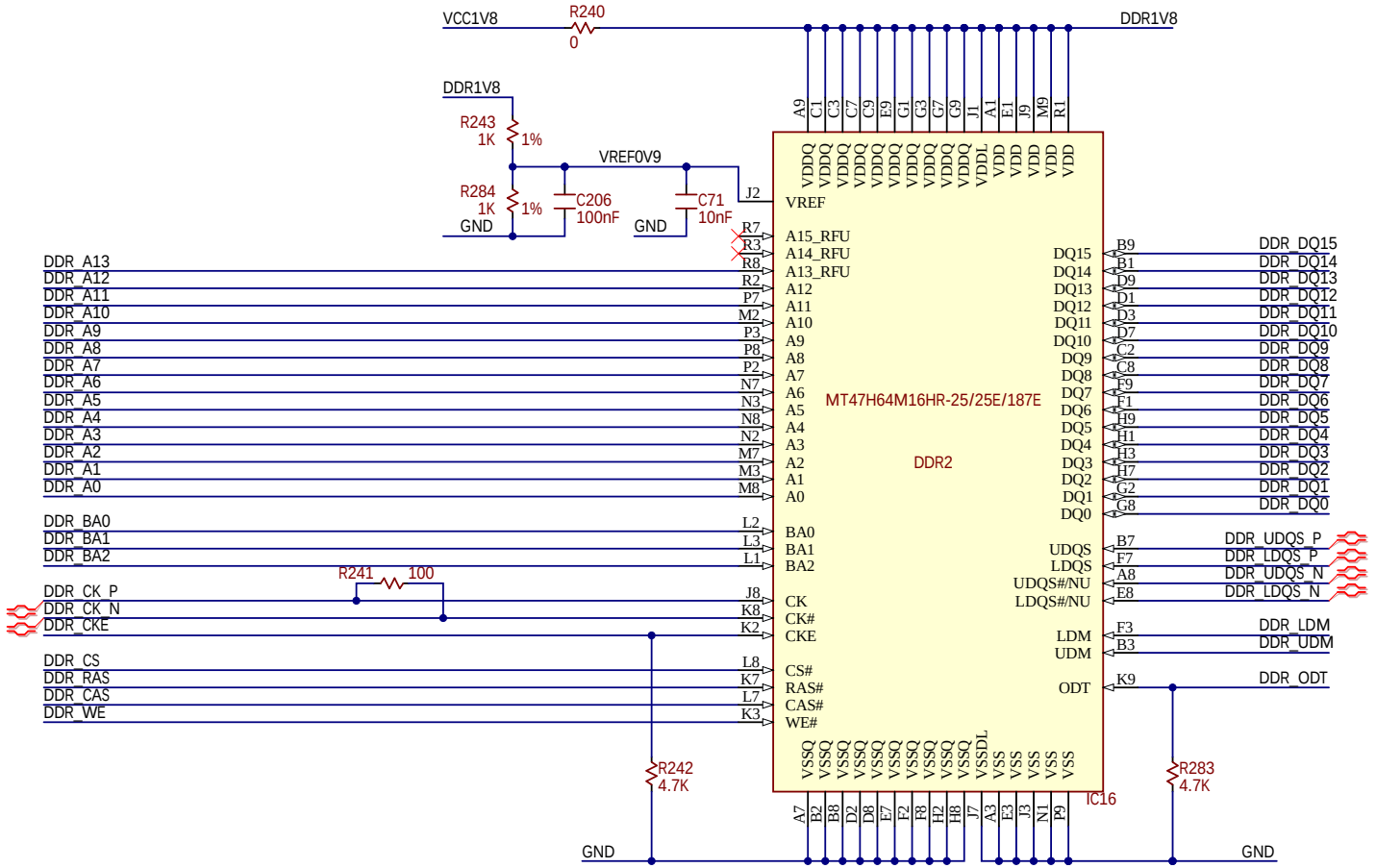

Title	Nexys A7
Rev	D.3
Circuit	DDR2 Memory
Doc#	500-292
Engineer	EG
Author	DL
Date	1/25/2022
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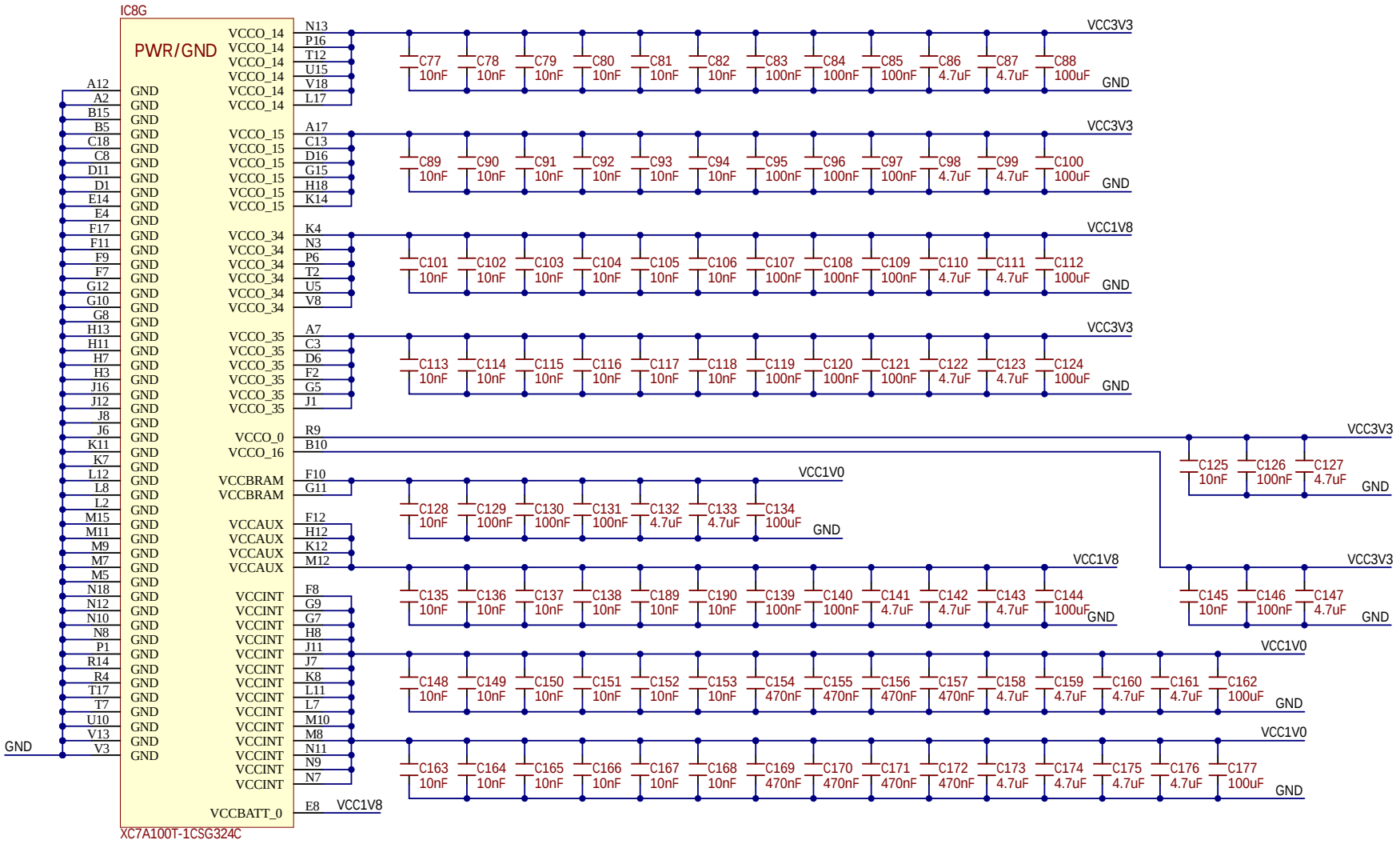

Title	Nexys A7
Rev	D.3
Circuit	FPGA POWER
Doc#	500-292
Engineer	EG
Author	DL
Date	1/25/2022
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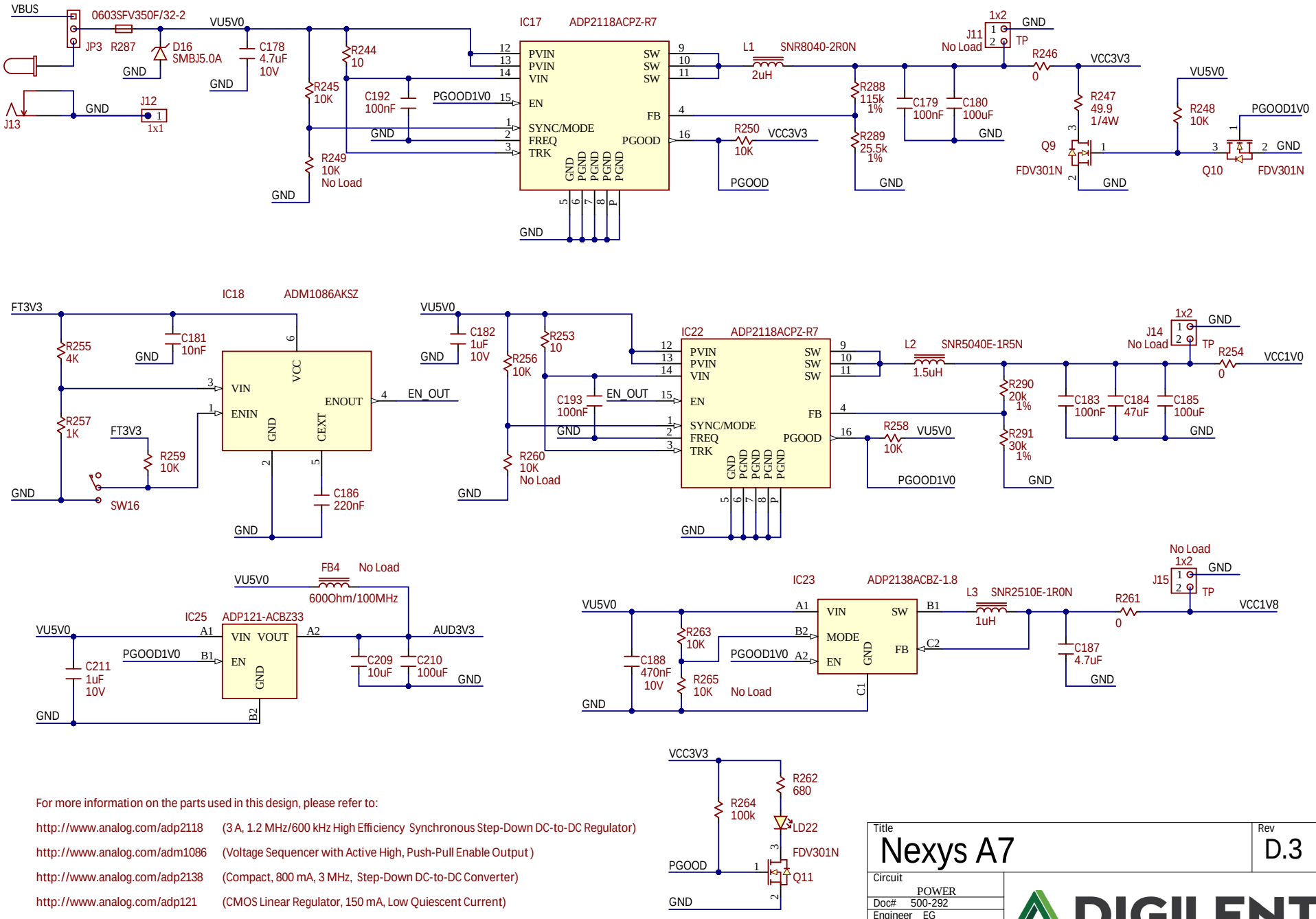

For more information on the parts used in this design, please refer to:

http://www.analog.com/adp2118 (3 A, 1.2 MHz/600 kHz High Efficiency Synchronous Step-Down DC-to-DC Regulator)

http://www.analog.com/adm1086 (Voltage Sequencer with Active High, Push-Pull Enable Output)

http://www.analog.com/adp2138 (Compact, 800 mA, 3 MHz, Step-Down DC-to-DC Converter)

http://www.analog.com/adp121 (CMOS Linear Regulator, 150 mA, Low Quiescent Current)

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